Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1 (canceled).

2 (currently amended). The adder circuit of claim ~~1~~ 3, wherein each generate bit is the logical AND of its corresponding bits in the first and second operand, each propagate bit is the EXOR of its corresponding bits in the first and second operands, and each kill bits is the logical NOR of its corresponding bits in the first and second operands.

3 (currently amended). ~~The adder circuit of claim 1,~~ **An adder circuit for determining the sum of two operands, comprising:**

a set of PGK circuits configured to generate propagate, generate, and kill bits corresponding to at least a portion of the first and second operands;

at least one tier of group circuits configured to receive the propagate, generate, and kill bits from a plurality of the PGK circuits and to produce, in response thereto, a set of group propagate, generate, and kill values;

a carry generation circuit configured to receive a carry-in bit and the outputs of at least one of the group circuits and further configured to generate a carry-out bit representing the carry-out of the corresponding group; and

a select circuit configured to select between a first sum and a second sum responsive to the carry-out bit;

wherein at least one of the PGK circuits, group circuits, and carry circuits includes at least one CMOS transmission gate.

4-7 (canceled).

8 (currently amended). The adder circuit of claim ~~1~~ 3, wherein the at least one tier of group circuits includes a first tier of group circuits configured to receive the output of the PGK circuits and to generate an intermediate set of group propagate, generate, and kill values, and a second tier of at least one group circuit configured to receive the intermediate set of group propagate, generate, and kill values and to produce a final group propagate, generate, and kill values.

9 (original). The adder circuit of claim 8, wherein the intermediate group of propagate, generate, and kill values each corresponds to a group of four adjacent bits and further wherein the final group of propagate, generate, and kill values correspond to a group of 16 adjacent bits.

10 (canceled).

11 (canceled).

12 (currently amended). The microprocessor of claim ~~11~~ 13, wherein each generate bit is the logical AND of its corresponding bits in the first and second operand, each propagate bit is the EXOR of its corresponding bits in the first and second operands, and each kill ~~bits~~ bit is the logical NOR of its corresponding bits in the first and second operands.

13 (currently amended). ~~The microprocessor of claim 11,~~ **A microprocessor including and adder circuit for determining the sum of two operands, the adder comprising:**

a set of PGK circuits configured to generate propagate, generate, and kill bits corresponding to at least a portion of the first and second operands;

at least one tier of group circuits configured to receive the propagate, generate, and kill bits from a plurality of the PGK circuits and to produce, in response thereto, a set of group propagate, generate, and kill values;

a carry generation circuit configured to receive a carry-in bit and the outputs of at least one of the group circuits and further configured to generate a carry-out bit representing the carry-out of the corresponding group; and

a select circuit configured to select between a first sum and a second sum responsive to the carry-out bit

wherein at least one of the PGK circuits, group circuits, and carry circuits includes at least one CMOS transmission gate.

14 (canceled).

15 (currently amended). The microprocessor of claim ~~11~~ 13, wherein the PGK circuits further generate the logical complements of the propagate, generate, and kill bits substantially simultaneously with the generation of the propagate, generate, and kill bits.

16 (original). The microprocessor of claim 15, wherein the group circuits further generate the logical complements of the group propagate, generate, and kill values substantially simultaneously with the generation of the group propagate, generate, and kill values.

17 (canceled).

18 (currently amended). The microprocessor of claim ~~11~~ 13, wherein the at least one tier of group circuits includes a first tier of group circuits configured to receive the output of the PGK circuits and to generate an intermediate set of group propagate, generate, and kill values, and a second tier of at least one group circuit configured to receive the intermediate set of group propagate, generate, and kill values and to produce a final group propagate, generate, and kill values.

19 (original). The microprocessor of claim 18, wherein the intermediate group of propagate, generate, and kill values each corresponds to a group of four adjacent bits and further wherein the final group of propagate, generate, and kill values correspond to a group of 16 adjacent bits.

20 (canceled).

21 (newly inserted). The adder circuit of claim 3, wherein the CMOS transmission circuit comprises a PMOS transistor and an NMOS transistor, wherein a first source/drain terminal of the PMOS transistor is connected to a first source/drain terminal of the NMOS transistor and wherein a second source/drain terminal of the PMOS transistor is connected to a second source/drain terminal of the NMOS transistor.

22 (newly inserted). The adder circuit of claim 21, wherein a gate terminal of the PMOS transistor is driven by a first signal and a gate terminal of the NMOS transistor is driven by the logical complement of the first signal.

23 (newly inserted). The adder circuit of claim 22, wherein at least one of the PGK circuits includes a propagate circuit having a first CMOS transmission gate receiving a first input signal that is gated by the inverse of a second input signal and a second CMOS transmission gate receiving an inverse of the first input signal that is gated by the second input signal.

24 (newly inserted). The adder circuit of claim 22, wherein a group circuit includes a group generate circuit, a group propagate circuit, and a group kill circuit, each comprising a plurality of CMOS transmission gates connected in series with source/drain terminals of a first transmission gate connected to source/drain terminals of the next.

25 (newly inserted). The adder circuit of claim 24, wherein each transmission gate is controlled by one of the propagate bits.